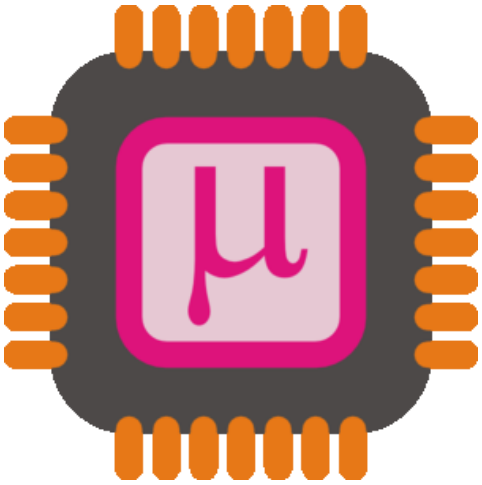
Darbhanga College of Engineering

COURSE FILE

OF

Microprocessor and Its Applications

(EEUG 6 031611)



Faculty Name:

Mr. AMIT KUMAR

ASSISTANT PROFESSOR, DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

विज्ञान एवं प्रावैधिकी विभाग
Department of Science and Technology
Government of Bihar

CONTENTS

Vision of EEE Dept.-

To produce quality electrical and electronics engineers to pursue higher studies, serve the national, multi-national companies and society at large.

Mission of EEE Dept.:-

M1: To provide high quality teaching and finest environment for learning to the students.

M2: To promote the graduates for higher studies and research

M3: To embed ethical values in graduates through various activities.

M4: To expose our graduates to the latest technology and research through collaboration with the industry and research institutes.

EEE Engineering Program Educational Objectives

After 4 to 5 years of graduation a BE (EEE) graduate would be able to

PSO 1. Students should be able to identify, formulate and solve problems in the areas of automation, control systems and power engineering.
PSO 2. Students will be able to provide sustainable solutions to growing energy demands.

PEO 1. The graduate will apply the electrical and electronics engineering concepts to excel in higher education and research & development activity having strong foundation in science and technology.
PEO 2. The graduate will demonstrate the knowledge and skills to solve real life engineering problems and design electrical systems that are technically sound, economical and socially acceptable.
PEO 3. The graduates will showcase the professional skills keeping team spirit, societal and ethical values.

EEE Engineering Student Outcomes

Students who complete the B.E. Degree in EE will be able to:

1. Fundamental knowledge and exposure to basic sciences to support the core (Electrical) engineering stream.
2. Skill development and knowledge to use the mathematics and other basic sciences as a tool for the core (Electrical) engineering program.
3. Knowledge and exposure to other engineering sciences and social sciences, aiding the program core (Electrical) with due consideration to interdisciplinary intricacies.
4. To develop skills to analyze the core (Electrical) engineering problems, through experimentation and analysis.
5. To develop the "understanding and the skills" needed to analyze core (Electrical) engineering problems which are complex and need to be learnt through scaled down lab-models, or simulations (Computer based). Development of soft skills to aid the core engineering discipline.
6. To give basic understanding of economic, social, legal and safety issues associated with core (Electrical)engineering discipline.
7. To impart knowledge related to renewable energy sources and energy conservation issues, point towards sustainable development, though the core (Electrical) engineering discipline.
8. To impart knowledge related to professional practices applicable to engineering practices.

9. Personality development to work in groups required for the system science related complex problems with multidisciplinary knowledge requirement through the program specific electives.
10. To impart knowledge required for effective professional communications through technical writing, reports and presentations.
11. Skill development and knowledge in the area of core engineering activates (Electrical, Electronics, Power and Control) specific to the program.
12. To impart education to learn over and above the planned curriculum leading self and lifelong learning habits.

Course Description

The microprocessor and microcontrollers are the most useful electronic chips, which are used to design and develop processor and computer based automatic smart electronics systems for home and industry application. Students learn CPU architecture, memory interfaces and management, coprocessor interfaces, bus concepts, bus arbitration techniques, interfacing of systems using AD/DA, serial I/O devices, DMA, interrupt control devices, including design, construction, and testing of dedicated microprocessor systems (static and real-time). Upon completion, students should be able to design, construct, program, verify, analyze, and troubleshoot fundamental microprocessor interface and control circuits using related equipment.

Course Objectives

1. The objective of this course is to become familiar with the architecture and the instruction set of an Intel microprocessor
2. To gain an in-depth understanding of the operation of microprocessors and microcontrollers, machine language programming & interfacing techniques with peripheral devices.
3. Assembly language programming will be studied as well as the design of various types of digital and analog interfaces
4. To learn the concept of designing computer organization and architecture.
5. To gain an understanding of applications of microprocessors in designing processor-based automated electronic system.

Course Outcomes (Students are able to)

1. Understand the architecture, working and operations of the microprocessors.
2. Analyze the fetching of data, address and the basic programming using assembly language in order to digitize the world.
3. Evaluate the usage of microprocessor and its interfacing with peripheral devices.
4. Understand and apply the usage of microcontroller to execute small and specific objective programs.
5. Create some programs helping in daily life based on microprocessor-8085 and microcontroller-8086.

CO-PO MAPPING

PSO 1. An ability to identify, formulate and solve problems in the areas of Electrical and Electronics Engineering.

PSO 2. An ability to use the techniques, skills and modern engineering tools necessary for innovation.

Sr. No.	Course Outcome	PO
1.	**031611.1** Understand the architecture, working and operations of the microprocessors.	PO1, PO4, PO5, PO6, PO7
2.	**031611.2** Analyze the fetching of data, address and the basic programming using assembly language in order to digitize the world.	PO1, PO2, PO3, PO4, PO5, PO6
3.	**031611.3** Evaluate the usage of microprocessor and its interfacing with peripheral devices.	PO1, PO2, PO3, PO4, PO5, PO9
4.	**031611.4** Understand and apply the usage of microcontroller to execute small and specific objective programs.	PO1, PO2, PO3, PO4, PO5, PO6, PO8, PO9, PO11, PO12,PSO1, PSO2
5.	**031611.5** Create some programs helping in daily life based on microprocessor-8085 and microcontroller-8086.	PO1, PO2, PO3, PO4, PO5, PO6, PO7,PO8, PO9, PO11, PO12,PSO1, PSO2

Course Outcomes	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
	Engineering knowledge	Problem analysis	Design/development of solutions	Investigation	Modern tool usage	The engineer and society	Environment and sustainability	Ethics	Individual and team work	Communications	Project management and finance	Life-long learning		
031611.1 Understand the architecture, working and operations of the microprocessors.	3			1	1	1	1							
031611.2 Analyze the fetching of data, address and the basic programming using assembly language in order to digitize the world.	2	2	2	2	2	1								

031611.3 Evaluate the usage of microprocessor and its interfacing with peripheral devices.	2	2	2	1	1				2					
031611.4 Understand and apply the usage of microcontroller to execute small and specific objective programs.	3	3	3	3	2	1		2	3		2	1	2	2
031611.5 Create some programs helping in daily life based on microprocessor-8085 and microcontroller-8086.	2	2	3	1	2	2	1	1	3		3	1	3	3

B. Tech. VI Semester (EEE)
031611 MICRO PROCESSOR AND ITS APPLICATION

L-T-P: 3-0-3 Credit: 5	Max Marks:	100
	Final Exam:	70 Marks
	Sessional:	20 Marks
	Internals:	10 Marks.

Intel 8085

1. **Introduction:** CPU, Register, memory, Buses, Memory addressing capacity of a CPU. **Lecture: 3**
2. **CPU Architecture,** Pin configuration, Instructions, Addressing modes, Instruction word size, Languages. **Lecture : 4**
3. **Timing Diagram:** Read cycle, write cycle, fetch cycle, Memory read, Memory write, I/O cycle. **Lecture : 3**
4. **Programming :** Simple programming : 8-bit addition &subtraction, 16-bit addition , Delay subroutine using register, finding lowest & highest no. in data array. **Lecture: 5**
5. **Data transfer** schemes, I/O port. **Lecture: 6**
6. **8255, 8251, 8253, 8257** chips, pin diagram, control word, operating modes. **Lecture: 6**
7. **Interfacing** to ADC, Analog multiplexer, simple & hold. **Lecture: 4**

Intel 8086

8. **Architecture:** BIU & Execution unit, pin diagram, function of different modes, registers. **Lecture: 4**
9. **Addressing Modes**, Instruction **Lecture : 4**
10. **Programming. Lecture: 3**

Text Books:

1. Fundamental of Microprocessor & Microcomputer by B.Ram, Dhanpat Rai
2. Advance Microprocessor by B.Ram

Reference Books:

1. Microprocessor & Interfacing by D.V hall,TMH
2. Microprocessor Architecture by R.S Gaonkar
3. Microprocessor with Application in process control by S.I Ahson. TMH
4. Programming Microprocessor Interfaces by Michael Andrews, PHI
5. The Intel Microprocessor Architecture, Programming & Interfacing by B.Brey, PHI

Microprocessor and its Applications

Data converters: sample and hold circuits, ADCs and DACs; Semiconductor memories: ROM, SRAM, DRAM; 8-bit microprocessor (8085): architecture, programming, memory and I/O interfacing.

DARBHANGA COLLEGE OF ENGINEERING, DARBHANGA **w.e.f. – 13-01-2020**

EEE Semester – 6th, Session (2017-21)

Day	Branch	1 (09am-10.00am)	2 (10.00am-11.00am)	3(11.00am-12.00pm)	4(12.00pm-1.00pm)	Lunch (1.00pm – 2.00pm)	5(2.00pm – 3.00pm)	6(3.00pm-4.00pm)	7(4.00pm-5.00pm)
Monday	E.E.E.								
Tuesday	E.E.E.				μ-P				
Wednesday	E.E.E.						μ-P		
Thursday	E.E.E.						μ-P Lab		
Friday	E.E.E.	μ-P					μ-P Lab		
Saturday	E.E.E.						μ-P (T)		

Mechanical – M1 - 1 to 30 **E.E.E.** - E1 - 1 to 30 **C. Sc.** - CS1 – 1 to30 **Civil** - C1 – 1 to 30
S-1 M2 –31 to All S-2 E2 – 31 to All S-3 CS2 – 31 to All B.C.R. C2 – 31 to All

Prof . Incharge Routine
D.C.E. Darbhanga

Principal
D.C.E., Darbhanga

Student List (2017-21)

Registration No.	Enrolment Number
17110111001	RAUSHAN MISHRA
17110111002	GULSHAN KUMAR
17110111003	ROSHAN KUMAR
17110111004	ARUNODAY LAL
17110111005	PRANTIKA SUMAN
17110111006	HIMANI
17110111007	CHANDAN KUMAR
17110111008	SUBHKANT SAHU
17110111009	SHAMIM AKHTAR
17110111010	AKSHAY KUMAR
17110111011	SUBHAM KUMAR
17110111012	PRITY SINHA
17110111013	FUDAN KUMAR
17110111014	JYOTI KUMARI
17110111015	GAURAV KUMAR
17110111016	ARVIND KUMAR
17110111017	GOVIND KUMAR
17110111018	KESHAV KUMAR
17110111019	MUNNA KUMAR
17110111020	ABHIJEET KUMAR

17110111021	AJAY RAJ
17110111022	DEEPIKA KUMARI
17110111023	LEEPI DAS
17110111024	VIKASH KUMAR
17110111025	UDAY KUMAR YADAV
17110111026	HEMANT KUMAR
17110111027	SHUBHAM KUMAR ANAND
17110111028	MD TAUHID
17110111029	MD ASIF
17110111031	AMAN KUMAR
17110111032	AMAN JAISWAL
17110111033	RAVI NAYAN KISHOR
17110111034	DILIP KUMAR
17110111035	ANIL KUMAR
17110111036	MD RAFIULLAH
17110111037	SHASHANK KUMAR
17110111038	SAKSHI SUMAN
17110111039	SUNIL KUMAR RAM
17110111041	RAHUL KUMAR
17110111042	SATYAM KUMAR
17110111043	DIPU KUMAR MISHRA
17110111044	VIKASH KUMAR
17110111045	SAROJ KUMAR

17110111046	AJAY KUMAR SINGH
17110111047	MD NAYEEM
17110111048	MD SHAMIM AKHTAR
17110111049	DEEPA KUMARI
17110111050	SUBHASH KUMAR
17110111051	PRIYA KUMARI
17110111052	AMRENDRA KUMAR
17110111053	RANI RUPA
17110111054	AMAN KUMAR SRIVASTVA
17110111055	ADITYA KUMAR
17110111056	RAUSHAN KUMAR RAM
17110111057	POOJA KUMARI
17110111058	AVINASH KUMAR MISHRA
17110111059	RAHUL KUMAR
17110111060	VARUN KUMAR

Institute / College Name :	Darbhanga College of Engineering		
Program Name	**B.Tech EEE**		
Course Code	EEUG 6 031611		
Course Name	Microprocessor and its Applications		
Lecture/Tutorial/Lab (per week):	3/0/3	**Course Credits**	5
Course Coordinator Name	Mr. Amit Kumar		

1. **Scope and Objectives of the Course**
   1. The objective of this course is to become familiar with the architecture and the instruction set of an Intel microprocessor
   2. To gain an in-depth understanding of the operation of microprocessors and microcontrollers, machine language programming & interfacing techniques with peripheral devices.
   3. Assembly language programming will be studied as well as the design of various types of digital and analog interfaces
   4. To learn the concept of designing computer organization and architecture.
   5. To gain an understanding of applications of microprocessors in designing processor-based automated electronic system.

2. **Textbooks**
   TB1: Fundamental of Microprocessor & Microcomputer by B.Ram, Dhanpat Rai
   TB2: Advance Microprocessor by B.Ram
3. **Reference Books**
   RB1: Microprocessor & Interfacing by D.V hall,TMH
   RB2: Microprocessor Architecture by R.S Gaonkar.
   RB3: Microprocessor with Application in process control by S.I Ahson. TMH
   RB4: Programming Microprocessor Interfaces by Michael Andrews, PHI
   RB5: The Intel Microprocessor Architecture, Programming & Interfacing by B.Brey, PHI
   RB6: The 8051 Microcontroller and Embedded Systems: Using Assembly and C

Other readings and relevant websites

S.No.	**Link of Journals, Magazines, websites and Research Papers**
1.	https://www.scribd.com/doc/40989017/Microprocessor-and-Applications-EC1303-Question-Bank
2.	http://www.nptel.ac.in/courses/Webcourse-contents/IIScBANG/Microprocessors%20and%20Microcontrollers/pdf/Question_Bank/QBm3.pdf
3.	https://www.journals.elsevier.com/microprocessors-and-microsystems/
4.	https://www.sciencedirect.com/journal/microprocessors-and-microsystems
5.	http://ieeexplore.ieee.org/document/1454516/

4. **Course Plan**

Lecture Number	Date of Lecture	Topics	Web Links for video lectures	Text Book / Reference Book / Other reading material	Page numbers of Text Book(s)
1-3		**Introduction:**		**TB1, RB1, RB2**	**1.11-1.32**
		CPU, Register, memory, Buses, Memory addressing capacity of a CPU	http://slideplayer.com/slide/5261625/		
Assignment I					
4-7		**CPU Architecture**		**TB1, RB1, RB2**	**3.1-3.15, 4.2- 4.4**
		Pin configuration, Instructions, Addressing modes, Instruction word size, Languages.	https://www.youtube.com/watch?v=p9wxyIx-j-c		
8-10		**Timing Diagram:**		**TB1, RB1, RB2**	**3.9- 3.15**
		Read cycle, write cycle, fetch	https://www.youtube.c		

		cycle, Memory read, Memory write, I/O cycle.	om/watch?v=JoHJL5CnFl8		
Assignment II					
11-15		**Programming :**		**TB1, RB1, RB2**	**6.1-6.64**
		Simple programming : 8-bit addition &subtraction, 16-bit addition , Delay subroutine using register, finding lowest & highest no. in data array.	https://www.youtube.com/watch?v=HXYhBCpDoVc		
Assignment III					
16-17		**Data transfer schemes**		**TB1, RB1, RB2**	**7.5-7.32**
		I/O port.	https://www.youtube.com/watch?v=3-C6Ob5cBZw		
18-21		**Pin Diagrams**		**TB1, RB1, RB2**	**11.1-11.12**
		8255, 8251, 8253, 8257 chips, pin diagram, control word, operating modes	https://www.youtube.com/watch?v=DrGdp7vo58A		
22-24		**Interfacing**		**TB1, RB1, RB2**	
		ADC, Analog multiplexer, simple & hold.	https://www.youtube.com/watch?v=nigEcGE2Ql0		
Assignment IV					
25-28		**Architecture : 8086**		**TB1, RB6**	**11.13-11.51**
		BIU & Execution unit, pin diagram, function of different modes, Registers	https://www.youtube.com/watch?v=DmwOSdwzZ3E		
Assignment V					
29-35		**Programming: 8086**		**TB1, RB6**	**11.53-11.60**
		Addressing Modes, Instruction Programming.	https://www.youtube.com/watch?v=cSniV2F94-I		

1. **Evaluation Scheme:**

Component 1	Mid Semester Exam	20
Component 2	Assignment Evaluation	10
Component 3**	End Term Examination**	70
	Total	**100**

** The End Term Comprehensive examination will be held at the end of semester. The mandatory requirement of 75% attendance in all theory classes is to be met for being eligible to appear in this component.

SYLLABUS

Topics	No of lectures	Weightage
Introduction : CPU, Register, memory, Buses, Memory addressing capacity of a CPU	3	9%
CPU Architecture, Pin configuration, Instructions, Addressing modes, Instruction word size, Languages.	4	11%
Timing Diagram: Read cycle, write cycle, fetch cycle, Memory read, Memory write, I/O cycle.	3	9%
Programming : Simple programming : 8-bit addition &subtraction, 16-bit addition , Delay subroutine using register, finding lowest & highest no. in data array.	5	14%
Data transfer schemes, I/O port.	2	6%
8255, 8251, 8253, 8257 chips, pin diagram, control word, operating modes.	4	11%
Interfacing to ADC, Analog multiplexer, simple & hold.	3	9%

Architecture : BIU & Execution unit, pin diagram, function of different modes, Registers	4	11%
Addressing Modes, Instruction Programming.	7	20%

This Document is approved by:

Designation	**Name**	**Signature**
Course Coordinator	Mr. Amit Kumar	
H.O.D	Mr. Prabhat Kumar	
Principal	Prof. Achintya	
Date	13-01-2020	

Evaluation and Examination Blue Print:
Internal assessment is done through quiz tests, presentations, assignments and project work. Two sets of question papers are asked from each faculty and out of these two, without the knowledge of faculty, one question paper is chosen for the concerned examination. Examination rules and regulations are uploaded on the student's portal. Evaluation is a very transparent process and the answer sheets of sessional tests, internal assessment assignments are returned back to the students.
The components of evaluations alongwith their weightage followed by the University is given below

Sessional Test 1	20%
Assignments/Quiz Tests/Seminars	10%
End term examination	70%

Course Outcomes
At the end of the course the student will be able to

1. Understand the architecture, working and operations of the microprocessors.
2. Analyze the fetching of data, address and the basic programming using assembly language in order to digitize the world.
3. Evaluate the usage of microprocessor and its interfacing with peripheral devices.
4. Understand and apply the usage of microcontroller to execute small and specific objective programs.
5. Create some programs helping in daily life based on microprocessor-8085 and microcontroller-8086.

Institute / School Name :	Darbhanga College of Engineering		
Program Name	**B.E. EEE**		
Course Code	EEUG 6 031611		
Course Name	Microprocessor and its Applications		
Lecture/Tutorial/Lab (per week):	3/0/3	**Course Credits**	5
Course Coordinator Name	Mr. AMIT KUMAR		

LECTURE PLAN

Topics	**Lecture Number**	**Date on which the Lecture was taken**
Introduction		
CPU, Register	**1**	
Memory, Buses,	**2**	
Memory addressing capacity of a CPU	**3**	
CPU Architecture		
Pin configuration	**4**	
Instructions	**5**	
Addressing modes	**6**	
Instruction word size, Languages.	**7**	
Timing Diagram:		
Read cycle, write cycle,	**8**	
fetch cycle, Memory read,	**9**	
Memory write, I/O cycle.	**10**	
Programming :		
Simple programming : 8-bit addition	**11**	
8-bit subtraction	**12**	
16-bit addition & Subtraction	**13**	
Delay subroutine using register	**14**	
finding lowest & highest no. in data array.	**15**	
Data transfer schemes		
Data Transfer schemes	**16**	
I/O port.	**17**	
Pin Diagrams		
8255 chips, pin diagram, control word, operating modes	**18**	
8251 chips, pin diagram, control word, operating modes	**19**	
8253 chips, pin diagram, control word, operating modes	**20**	
8257 chips, pin diagram, control word, operating modes	**21**	
Interfacing		
ADC	**22**	
Analog multiplexer	**23**	
simple & hold.	**24**	
Architecture : 8086		
BIU & Execution unit	**25**	
pin diagram	**26**	
function of different modes,	**27**	
Registers	**28**	
Programming: 8086		
Addressing Modes	**29-32**	
Instruction Programming.	**33-35**	

Darbhanga College of Engineering

Department of Electrical and Electronics Engineering

Microprocessor and its Applications
Assignment I

1. What is a Microprocessor? What is the difference between a Microprocessor & CPU
2. What determines that Microprocessor is an 8, 16 or 32 bit?
3. What are the advantages of an assembly language in comparison with high level languages?
4. How many memory locations can be addressed by a microprocessor with 14 address lines?
5. What is the function of the accumulator?
6. What is a flag?
7. **a)** Why are the program counter and the stack pointer 16-bit registers?

   b) Specify the number of registers and memory cells in a 128 x 4 memory chip.
8. What is the difference between INR & INX instructions?
9. **a)** Discuss various types of addressing modes of 8085.

   b) Define & explain the term addressing modes.
11. Draw and explain the block diagram of a microprocessor 8085.

Darbhanga College of Engineering

Department of Electrical and Electronics Engineering

Assignment 2

Microprocessor and Its Applications
Course Code: 031611

1. Differentiate between
   (a) Microcontroller, Microcomputer & Microprocessor
   (b) RISC & CISC Processor
   (c) RIM & SIM
   (d) Memory Mapped I/O Scheme and I/O Mapped I/O Scheme.

2. Draw and explain the timing diagram of MVI B, 07 H.
3. Discuss the operating principle of 8253.
4. Discuss the pin description of 8251.
5. Discuss the addressing modes of 8085 and 8086 microprocessor.
6. Discuss the operating modes of 8255.
7. Draw the Block Diagram of 8254 PPI (Programmable Peripheral Interface) and explain the various modes in which 8254 can operate and write down the control word for each mode. Specify the conditions to start the timer of 8254 PPI.
8. Draw the block diagram of 8257 DMA controller. Explain the working of 8257 along with the different modes in which 8257 can operate.
9. Draw and discuss the timing diagram of memory read cycle. Define and differentiate among T-state, machine cycle and instruction cycle.
10. Explain the following terms with respect to Sample and Hold circuits.
    (a) Acquisition Time
    (b) Aperture Time
    (c) Droop Time
    Also explain the parameters which should be considered while selecting the capacitor for sample and hold circuit.
11. Explain what is meant by STACK. Where is it used in INTEL 8086? Discuss the steps involved in executing CALL instruction in Intel 8086.
12. Draw and discuss the interfacing circuit of ADC 0800, analog multiplexer, SAMPLE and HOLD circuit for a microprocessor-based system.
13. Discuss the status flags of INTEL 8086.

Note: For Programming go through the lab manual already sent to you. Practice as many programs as you can. Like some of the common programs asked are:

1. Also, look for some specific program based on BCD.
2. Arrange a given array in ascending and descending order.
3. Find the largest and smallest number from a given array.
4. Addition and subtraction programs are very common, please go through it.
5. Produce a delay using subroutine function.

Tutorial Sheet

List of Programs (WAP)

1. Addition of Two 8-bit numbers using 8085 microprocessor kit.
2. Addition of Two 16-bit numbers using 8085 microprocessor kit.
3. Subtraction of Two 8-bit numbers using 8085 microprocessor kit.
4. Subtraction of Two 16-bit numbers using 8085 microprocessor kit.
5. Arrange the data array in ascending order using 8085 microprocessor kit.
6. Arrange the data array in descending order using 8085 microprocessor kit.
7. Find the 1's and 2's complement of an 8-bit number using 8085 microprocessor kit.
8. Addition of Two 8-bit numbers using 8086 microprocessor kit.

Darbhanga College of Engineering, Darbhanga

CSE Department

B.Tech [SEM VI (EEE)]

Mid. Sem Exam
(Session: 2019-20)
Course Code–031611

Microprocessor and Its Applications

Time: 2 Hours ***Max. Marks: 20***

Note: Attempt all questions. CO–Course Outcomes, BL–Bloom Level

S. No.	Questions	Marks	CO	BL
1.	Create the program for 8085-microprocessor to arrange the five 8-bit numbers in ascending order. The numbers are FE, 11, EF, 2C, 04. Store the outputs at the address location, starting from 2800 H. Consider the starting address location for inputs be 2700 H and for main program the starting address is 2600 H.	**5**	**CO5**	**L6**
2.	Apply the knowledge of PUSH and POP operation to illustrate the working of CALL and RETURN in Subroutine functions.	**3**	**CO2**	**L4**
3.	Calculate the time delay produced by the given subroutine function. If the clock period of the microprocessor is 420 ns. MVI B, FC LOOP DCR B JNZ LOOP RET	**3**	**CO4**	**L3**
4.	Explain the working of the 8085 microprocessor with the status flags.	**2**	**CO1**	**L1**
5.	Analyze the different addressing modes available with the microprocessor 8085. Explain with suitable examples.	**2**	**CO2**	**L4**
6.	Implement a program in 8085 to add two 8-bit decimal number and also store the result in decimal format at the address 2500H.	**3**	**CO4**	**L3**
7.	Briefly explains the basic building blocks of the 8085 microprocessor OR Draw the pin diagram of 8085 and label it.	**2**	**CO3**	**L5**

Note: (Please delete these notes before printing)

1. **Number of questions may vary.**
2. **If you want to give optional question then give an option in the same question having same CO.**
3. **Mark the BL (Bloom Level) as L1: Remember, L2: Understand, L3: Apply, L4: Analyze, L5: Evaluate and L6: Create**

Code : 031511

B.Tech 5th Semester Examination, 2016

Microprocessor & its Application

Time : 3 hours *Full Marks : 70*

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are Nine questions in this paper.

(iii) Attempt five questions in all.

*(iii) **Question No. 1 is Compulsory.***

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1. Differentiate between the following (any seven): 2×7=14
   - Microcontroller & Microprocessor.
   - High level and low level language.
   - RISC Processor and CISC Processor.
   - I/O Mapped I/O and Memory Mapped I/O.
   - Assembler and Cross Assembler.
   - CALL and JMP.
   - STAX and LDAX.
   - XTHL and PCHIL
   - RIM and SIM

2 (a) Draw and explain the architecture of 8086. Describe the function of queue in 8086. How does the queue speeds up processing? 6

(b) Discuss the addressing technique used in 8086 and explain the various addressing modes of 8086. 8

3. Draw the Block Diagram of 8254 PPI and explain the various modes in which 8254 can operate and write down the control word for each mode. Specify the conditions to start the timer of 8254 PPI. 14
4. Draw the block diagram of 8257 DMA controller. Explain the working of 8257 along with the different modes in which 8257 can operate. 14
5. Explain the different interrupts available in 8085 processor. What is the purpose of the instruction RIM and SIM? How the status of pending interrupts is checked? Assuming the microprocessor is completing an RST 7.5 interrupt request, check to see if RST. 6.5 is pending. If it is pending, enable RST 6.5 without affecting any other interrupts; otherwise, return to the main program. 14
6. The figure below shown an interfacing circuit using the 8255 PPI in mode 1. Port A is designed as the input port for a keybord with interrupt I/O, and port B is designed as the output port for a printer with status check I/O. For the the given interfacing circuit do the following: 14

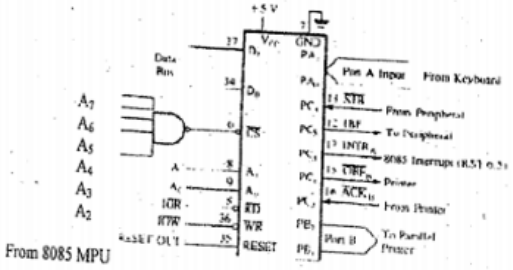
(a) Find port addresses by analyzing the decode logic.

(b) Determine the control word to set up port A as input and port B as output in mode 1.

(c) Determine the BSR word to enable $INTE_A$(port A).

(d) Determine the masking byte to verify the $\overline{OBF_B}$ line in the status check I/O (port B).

(e) Write initialization instructions and a printer subroutine to output characters that are stored in memory.



Figure

***

7. A set of ten packed BCD numbers is stored in the memory location. Write a program to add these number in BCD, if carry is generated wave it in register B, and adjust it for BCD. Write a subroutine to unpack the stored BCD sum and store it in two consecutive memory locations. 14
8. Two sets of three readings each are stored in memory. Write a program and draw the flowchart to sort the reading in descending order, assuming that the two sets are separated by word FFH. 14
9. Write a program to insert a string of four characters from the tenth location in the given array of 50 characters. 14

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Question Bank

Question1. What Are The Various Registers In 8085?

Answer :Accumulator register, Temporary register, Instruction register, Stack Pointer, Program Counter are the various registers in 8085.

Question2. What Are The Various Flags Used In 8085?

Answer :Sign flag, Zero flag, Auxillary flag, Parity flag, Carry flag.

Question3. What Is Stack Pointer?

Answer :Stack pointer is a special purpose 16-bit register in the Microprocessor, which holds the address of the top of the stack.

Question4. What Is Program Counter?

Answer :Program counter holds the address of either the first byte of the next instruction to be fetched for execution or the address of the next byte of a multi byte instruction, which has not been completely fetched.In both the cases it gets incremented automatically one by one as the instruction bytes get fetched. Also Program register keeps the address of the next instruction.

Question5. Which Stack Is Used In 8085?

Answer :LIFO (Last In First Out) stack is used in 8085.In this type of Stack the last stored information can be retrieved first.

Question6. What Happens When Hlt Instruction Is Executed In Processor?

Answer :The Micro Processor enters into Halt-State and the buses are tri-stated.

Question7. What Is Meant By A Bus?

Answer :A bus is a group of conducting lines that carriers data, address, & control signals.

Question8. What Is Tri-state Logic?

Answer :Three Logic Levels are used and they are High, Low, High impedance state. The high and low are normal logic levels & high impedance state is electrical open circuit conditions. Tri-state logic has a third line called enable line.

Question9. Give An Example Of One Address Microprocessor?

Answer :8085 is a one address microprocessor.

Question10. In What Way Interrupts Are Classified In 8085?

Answer :In 8085 the interrupts are classified as Hardware and Software interrupts.

Question11. What Are Hardware Interrupts?

Answer :TRAP, RST7.5, RST6.5, RST5.5, INTR.

Question12. What Are Software Interrupts?

Answer :RST0, RST1, RST2, RST3, RST4, RST5, RST6, RST7.

Question13. Which Interrupt Has The Highest Priority?

Answer :TRAP has the highest priority.

Question14. Name 5 Different Addressing Modes?

Answer :Immediate, Direct, Register, Register indirect, Implied addressing modes.

Question15. How Many Interrupts Are There In 8085?

Answer :There are 12 interrupts in 8085.

Question16. In 8085 Which Is Called As High Order / Low Order Register?

Answer :Flag is called as Low order register & Accumulator is called as High order Register.

Question17. What Are Input & Output Devices?

Answer :Keyboards, Floppy disk are the examples of input devices. Printer, LED / LCD display, CRT Monitor are the examples of output devices.

Question18. Can An Rc Circuit Be Used As Clock Source For 8085?

Answer :Yes, it can be used, if an accurate clock frequency is not required. Also, the component cost is low compared to LC or Crystal.

Question19. Why Crystal Is A Preferred Clock Source?

Answer :Because of high stability, large Q (Quality Factor) & the frequency that doesn't drift with aging. Crystal is used as a clock source most of the times.

Question20. What Does Quality Factor Mean?

Answer :The Quality factor is also defined, as Q. So it is a number, which reflects the lossness of a circuit. Higher the Q, the lower are the losses.

Question21. What Are Level-triggering Interrupt?

Answer :RST 6.5 & RST 5.5 are level-triggering interrupts

Question22. How Can Signals Be Classified For The 8085 Microprocessor?

Answer :The signals of the 8085 microprocessor based on their functions can be classified into 7 categories namely:

Frequency and power signals

Address and data buses

The control bus

Interrupt Signals

Serial Input / Output signals

DMA signals

Reset Signals

Question23. Mention The Various Functional Blocks Of The 8085 Microprocessor.?

Answer :The various functional blocks of the 8085 microprocessor are:

Registers

Arithmetic logic unit

Address buffer

Increment / decrement address latch

Interrupt control

Serial I/O control

Timing and control circuitry

Instructions decoder and machine cycle encoder.

Question24. Mention The Steps In The Interrupt Driven Mode Of Data Transfer.?

Answer :The steps followed in this type of transfer are as follows:

The peripheral device would request for an interrupt.

The request acknowledgement for the transfer is issued at the end of instruction execution.

Now the ISS routine is initialized, The PC has the return address which is now stored in the stack.Now data transfer is managed and coordinates by the ISS.

Again the Interrupt system is enabled and the above steps are repeated.

Question25. Write A Program That Will Store The Contents Of An Accumulator And Flag Register At Locations 2000h And 2001h.?

Answer :By making use of the Push & Pop instructions the program can be written as:

LXISP, 4000H - this step initiates the SP at 4000h.

PUSH PSW - the contents of the accumulator and flag are pushed into the stack.

POP B

MOV A, B

STA 2000H

MOV A, C

STA 2001H

HLT

Question26. Classify Interrupts On The Basis Of Signals. State Their Differences.?

Answer :On the basis of level the signals can be classified into the following types:

Single level interrupts

Multi level interrupts

The differences between them are as follows:

For single the interrupts are manages through a single ping whereas in multi they are managed by multiple pins.

For single level interrupts polling is essential whereas for multi level it is not necessary.

Single level interrupts are much slower than multi level interrupts.

Question27. What Are The Two Major Differences Between Intr And Other Interrupts (Hardware)?

Answer :The two major differences between INTR and the other hardware interrupts are as follows:All the hardware interrupts are vectored interrupts but the INTR interrupt is not so. An INTR interrupt will always get the address of a subroutine from the device (external) itself. In the case of other hardware interrupts the interrupts come from the call generated by the processor at a already determined vector location.

In case of the INTR interrupt the return address of an interrupt is never saved but in the case of other hardware interrupts the locations is saved in the stack.

Question28. Explain Briefly The Trap Input For The 8085.?

Answer :The TRAP input is sensitive to both edge and level.

The pulse width for this signal should be in excess as compared to the normal noise width.

A second trap will never be able to respond for the second time as it requires the first trap to go through a high to low transition.

The pulse widths are wider than normal widths so as to prevent unwanted false triggers.

Question29. Explain Briefly What Happens When The Intr Signal Goes High In The 8085?

Answer :The INTR is a maskable interrupt for the 8085. It has the lowest priority and is also non vectored. When this INTR signal goes into the high state the following things occur / take place:

For every instruction that is executed the 8085 checks the status of this interrupt./Till an instruction is completed the signal of INTR will remain high. Once an instruction is completed the processor sends an acknowledgement signal INTA. As soon as the INTA signal goes low a new opcode is placed on the data bus for transfer.

Once the new instruction is received the processor saves the address of new instruction into the STACK and an interrupt service subroutine begins.

Question30. Explain All The Addressing Modes Of The 8085 With The Help Of Examples.?

Answer :The various types of addressing modes of the 8085 are as follows:

Direct addressing: The instructions in itself contain the opearand. For ex. STA5513H or in/out instructions such as IN PORT C.

Register addressing: The general purpose registers contain the operands. For ex. MOV A, B;

Register indirect addressing: This involves the use of register pairs instead of a single register. For ex MOV A, M; ADD M.

Immediate addressing: The example are MVI A, 07; or ADI 0F etc.

Implicit addressing: this form of addressing contains no operands. For ex. RAR, CMA etc.

Question31. Mention The Different Types Of Data Transfers Possible In The 8085.?

Answer :The various types of data transfer operations possible are:

Data transfer is possible between two registers.

It is also possible between a memory location and a register.

Also it can occur between an input/output device and an accumulator.

In reality data is never transferred it can only be copied from one location to another.

Question32. What Differences Can You State Between The Hlt And Hold States?

Answer :The Hold is a hardware input whereas HLT is a software instruction.

When the HLT state is executed the processor simply stops and the buses are driven to tri state. No form of acknowledgement signal is given out by the processor.

In case of HOLD the processor goes into hold state but the buses are not driven to tri state.

When the processor goes into the HOLD state it gives out an HLDA signal. This signal can be made to use by other devices.

Question33. Does The 8085 Support Externally Initiated Operations? If Yes How?

Answer :Yes the 8085 does support several externally initiated operations. The possible operations and the corresponding pins for them in the 8085 are as follows:

It supports resetting (this is possible with the Reset Pin).

Various interruptions (these are possible through Trap, RST 7.5, 6.5, 5.5 and the interrupt pins.)

The 8085 also supports Readying with the help pf the Ready pin.

It also has a HOLD pin which can basically pause the operation till required/ as required.

Question34. Explain The Flow Of A Typical Instruction Word.?

Answer :The flow of a typical Instruction word is as follows:

The content of the program counter of 2 byte is transferred to the address register known as MAR (memory address register). This occurs at the starting of a fetch cycle.

The contents are transferred via the address bus.

Once this is done the timing and control section of the processor reads the contents of the referenced memory address location.

After this the data is sent to the memory data register with the help of the data bus.

Now the data is placed in the instruction register which will eventually decode and execute it.

Question35. Briefly Explain The Steps Involved In A Fetch Cycle.?

Answer :Fetch cycle is the time required to fetch an opcode from a particular location in memory.

General Fetch Cycles consist of 3T states.

The first T state involves the sending of the memory address stored in the Program Counter to the memory.

During the second T state the contents of the addressed memory is read (this generally is the opcode at the specified location)

In the third T state the opcode is sent to the Instruction register through the data bus for execution.

For slower memories the processors has the provision to get in to the WAIT cycles as well.

Question36. What Are Wait States In Microprocessors, Explain.?

Answer :The WAIT state plays a significant role in preventing CPU speed incompatibilities.

Many a times the processor is at a ready state to accept data from a device or location, but there might be no input available. This can lead to wastage of cpu time.

So in such cases when the cpu is ready for an input but there is no such valid data then the system gets into WAIT state. In this scenario the pin 35 (ready pin)is put into a low state.

As soon as there is some valid data for the 8085 the system comes off the WAIT state and the low state of the READY pin is withdrawn.

Question37. What Are The Boons And Banes Of Having More General Purpose Registers In A Microprocessor.?

Answer :If there are more general purpose registers the program writing process is more flexible and convenient.

The number of bits that would be required to detect the registers would increase with more registers, this results in the lowering of the number of operations.

When a program would involve CALL subroutines the status of the registers would have to be saved and restored often, this would result in a significant overhead for the processor.

Higher the number of these registers mores space would be used by them on the chip. This can create problems in adding / implementing other functions on the chip.

Question38. Explain In Brief The Control And Timing Circuitry Of The 8085.?

Answer :The timing and control circuitry section of the 8085 is responsible for the generation of timing and control signals so that instructions can be executed.

The types of signals involved are : Clock signals, Control signals, Status signals, DMA signals and also the reset section.

It is responsible for the fetching and the decoding of the various operations.

This section also aids in the generations of control signals for the executions of instructions and for the sync between external devices.

Question39. Explain Briefly The Flag Register In The 8085 Microprocessor.?

Answer :The flag register in 8085 is an 8-bit register which contains 5 bit positions.

These five flags are of 1bit F/F and are known as zero, sign, carry, parity and auxiliary carry.

For sign flag if the result of an MSB operation is 1 then it is set else it is reset.

The zero flag is set of the result of an instruction is zero.

The auxiliary carry flag is used for BCD operations, not free to the programmer.

The carry flag is used for carrying and borrowing in case of addition and subtraction operations.

The parity flag is used for results containing an even number of one's.

Question40. What Is A Stack Pointer Register, Describe Briefly.?

Answer :The Stack pointer is a sixteen bit register used to point at the stack.

In read write memory the locations at which temporary data and return addresses are stored is known as the stack.

In simple words stack acts like an auto decrement facility in the system.

The initialization of the stack top is done with the help of an instruction LXI SP.

In order to avoid program crashes a program should always be written at one end and initialized at the other.

Question41. Describe Briefly The Accumulator Register Of 8085.?

Answer :It is one of the most important 8 bit register of 8085

It is responsible for coordinating input and output to and from the microprocessor through it.

The primary purpose of this register is to store temporary data and for the placement of final values of arithmetic and logical operations.

This accumulator register is mainly used for arithmetic, logical, store and rotate operations.

Name of Faculty:- **Branch:-EEE**

Course Code:- **031611** **Section:-I**

Date of exam:-10-07-18

Test Type:- Internal

Test Abbrevation:SESSIONAL TEST

Maximum Marks 20

Test Topic:-Microprocessor and its Applications

Sr	Roll No.	Marks	% Marks
1	15103111124	6	27.5
2	15103111125	6	30
3	15103111126	1	5
4	15103111127	6	27.5
5	15103111128	16	77.5
6	15103111129	0	0
7	15103111130	1	5
8	15103111131	4	17.5
9	15103111132	7	35
10	15103111133	12	60
11	15103111134	8	40
12	15103111135	6	30
13	15103111136	15	75
14	15103111137	14	67.5
15	15103111138	10	47.5
16	15103111139	13	62.5
17	15103111141	6	27.5
18	15103111142	2	10
19	15103111143	6	27.5
20	15103111144	10	50
21	15103111145	5	25
22	15103111146	5	25
23	15103111147	10	47.5
24	15103111148	8	40
25	15103111149	9	45
26	15103111150	10	50
27	15103111151	5	25
28	15103111152	7	35
29	15103111153	3	15
30	15103111154	6	30
31	15103111155	11	52.5
32	15103111156	17	85
33	15103111157	2	7.5
34	15103111158	1	2.5
35	15103111159	17	82.5
36	15103111160	2	7.5
37	15103111161	3	15
38	15103111162	ABSENT	ABSENT
39	15103111163	6	27.5
40	15103111164	6	30
41	15103111165	2	7.5
42	15103111166	5	22.5
43	15103111168	16	77.5
44	15103111170	2	10
45	15103111171	7	32.5
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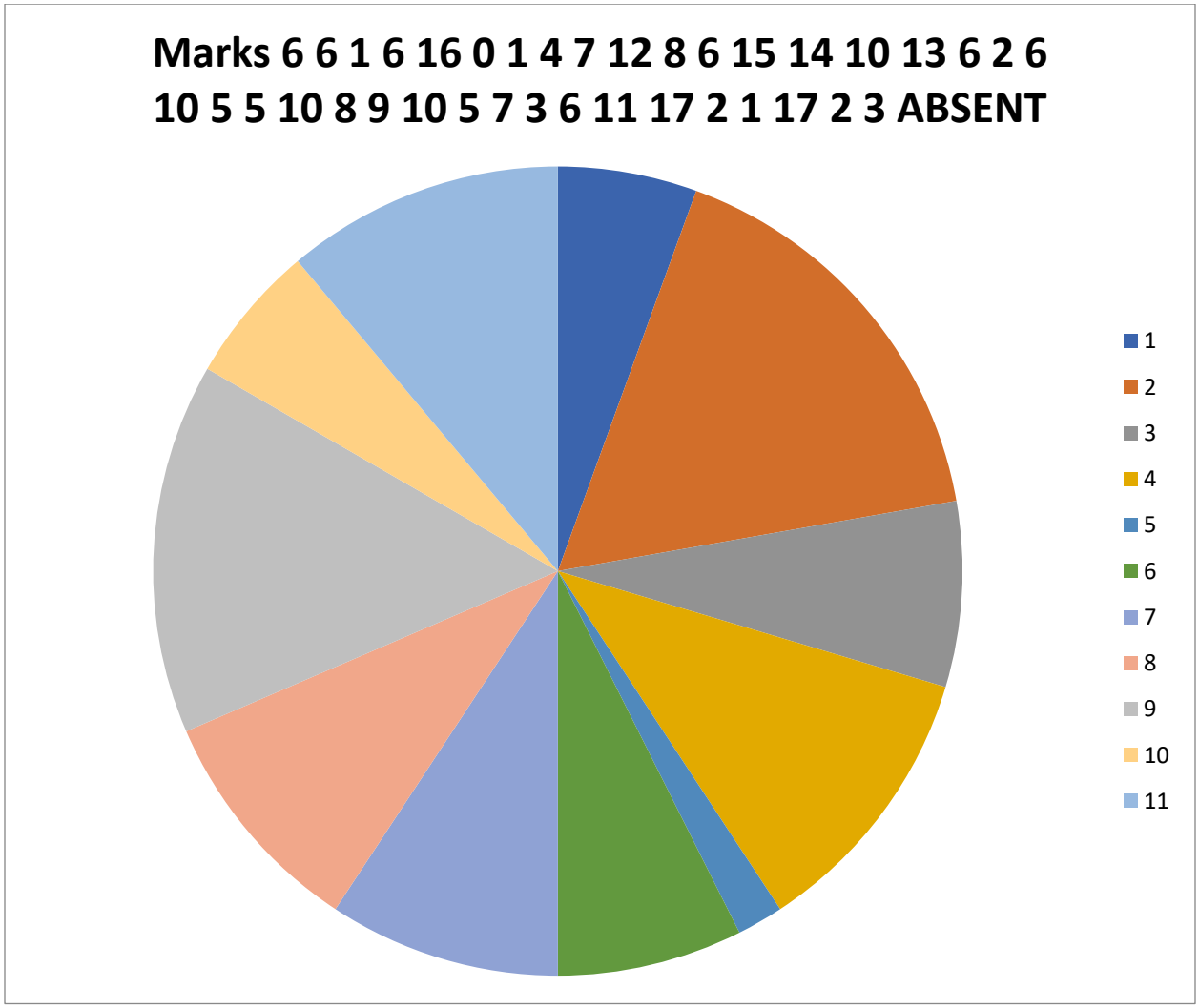
47	15103111173	10	47.5
48	15103111174	11	52.5
49	15103111175	11	55
50	15103111176	1	2.5
51	15103111177	2	10
52	15103111178	3	12.5
53	15103111179	3	12.5
54	15103111202	4	20
55	15103111208	13	65
56	15103111209	2	7.5
57	16110111901	6	27.5
58	16110111902	3	15

RESULT ANALYSIS



FAILED STUDENTS

Sr No.	Enrollement No.	Marks
1	15103111126	1
2	15103111129	0
3	15103111130	1
4	15103111131	4

5	15103111142	2
6	15103111153	3
7	15103111157	2
8	15103111158	1
9	15103111160	2
10	15103111161	3
11	15103111165	2
12	15103111166	5
13	15103111170	2
14	15103111172	3
15	15103111176	1
16	15103111177	2
17	15103111178	3
18	15103111179	3
19	15103111202	4
20	15103111209	2
21	16110111902	3

Quality Measurement Sheets

a. Course End Survey

ACADEMIC YEAR:	SEM:	DATE:
COURSE:	CLASS:	FACULTY:

Please evaluate on the following scale:

Excellent(E)	Good(G)	Average(A)	Poor(P)	No Comment(NC)
5	4	3	2	1

SNO	**QUESTIONAIRE**	**E 5**	**G 4**	**A 3**	**P 2**	**NC 1**	**Avg %**
GENERAL OBJECTIVES:							
1	Did the course achieve its stated objectives?						
2	Have you acquired the stated skills?						
3	Whether the syllabus content is adequate to achieve the objectives?						
4	Whether the instructor has helped you in acquiring the stated skills?						
5	Whether the instructor has given real life applications of the course?						
6	Whether tests, assignments, projects and grading were fair?						
7	The instructional approach (es) used was (were) appropriate to the course.						
8	The instructor motivated me to do my best work.						
9	I gave my best effort in this course						
10	To what extent you feel the course outcomes have been achieved.						
Please provide written comments:							

a) What was the most effective part of this course

b) What are your suggestions, if any, for changes that would improve this course?

c) Given all that you learned as a result of this course, what do you consider to be most important?

d) Do you have any additional comments or clarifications to make regarding your responses to any particular survey item?

e) Do you have any additional comments or suggestions that go beyond issues addressed on this survey?

TEACHING EVALUATION

COLLEGE NAME: DCE Darbhanga

Department of Electrical and Electronics Engineering

Course Assessment

ACADEMIC YEAR:	SEM:	DATE:
COURSE:	CLASS:	FACULTY:

Assessment	**Criteria Used**	**Attainment Level**			**Remarks**
Direct (d)	**Theory**				
	External Marks	___			
	Internal Marks (Theory)				
	Assignments				
	Tutorials				
Indirect (id)	**Course End Survey**				
Theory: Course Assessment (0.6 × d+ 0.4 × id)					

DARBHANGA COLLEGE OF ENGINEERING, DARBHANGA

6th Sem. Branch – Electrical & Electronics Engg. Batch (2015-19)

									CO 5	CO 2	CO 4	CO 1	CO 2	CO 4	CO 3		CO 1	CO 2	CO 3	CO 4	CO 5
S.No.	Name	E-MAIL	Mobile	Registration Number	Quiz/Assisn gment	External Marks	Mid sem	Total	q1	q2	q3	q4	q5	q6	q7		After adding all marks of a particular Cos				
					10	70	20		5	3	3	2	2	3	2		2	5	2	6	5
1	Puja Kumari	Puja12014@gmail.com	9431555074	15103111124	8	33	6		2			0.5	1.5	0.5	1		0.5	1.5	1	0.5	2
2	Mukul Raj	Mukulraj17869@gmail.com	7091981177	15103111125	8	25	6		1	0.5	0.5	1	1	2			1	1.5	0	2.5	1
3	Sushil Kumar Paswan	Sushilkumarpaswan0203@gmail.com	8199259142	15103111126	9	25	1		0.5					0.5			0	0	0	0.5	0.5
4	Ladly Kumari	laddlykumarising@gmail.com	7254855454	15103111127	8	34	6			1	1.5	1.5	0.5	0.5	0.5		1.5	1.5	0.5	2	0
5	Ayesha Jahan	AyeshaJahan775@gmail.com	7070520859	15103111128	10	32	16		3	3	1.5	2	2	2.5	1.5		2	5	1.5	4	3
6	Vikash Ranjan	VikashRanjanktr007@gmail.com	7979744090	15103111129	10	29	0		0	0	0	0	0	0	0		0	0	0	0	0
7	Raushan Kumar	Raushankumar7198@gmail.com	9199519998	15103111130	8	33	1						1				0	1	0	0	0
8	Anand Raj	laanandraj@gmail.com	8651441086	15103111131	10	32	4						1.5	0.5	1.5		0	1.5	1.5	0.5	0
9	Deepak Kumar	Dkumar930851@gmail.com	9608331653	15103111132	10	42	7		0.5	0.5	3	1.5	0.5	0.5	0.5		1.5	1	0.5	3.5	0.5
10	Nidhi	Nidhisrivastava203@gmail.com	8292534171	15103111133	9	47	12		2	2		2	2	2	2		2	4	2	2	2
11	Sunny Kant Raj	Sunny.k3698@gmail.com	8409879273	15103111134	10	49	8			2		1	1	2	2		1	3	2	2	0
12	Ravi Ranjan Kumar	Raviranjan8202@gmail.com	9155468054	15103111135	8	38	6		0	1	0	0	1	2.5	1.5		0	2	1.5	2.5	0
13	Nishant Saurabh	Nishant.d5594@gmail.com	9801622953	15103111136	10	47	15		4	2	3	2	2	1	1		2	4	1	4	4
14	Ajeet Kumar Pandit	Ajeetkp44@gmail.com	7061191490	15103111137	10	46	14		4	1.5	2	1	1.5	2.5	1		1	3	1	4.5	4
15	Prince Kumar	Prince803306@gmail.com	8676848429	15103111138	9	40	10		4.5	1	1	1	1	1			1	2	0	2	4.5
16	Vivek Kumar	Kv99roshan@gmail.com	9661936264	15103111139	10	51	13		4.5	1	1.5	1	1.5	1.5	1.5		1	2.5	1.5	3	4.5
17	Jalandhar Kumar Nishad	Kumarjkn9097042245@gmail.com	9097042245	15103111141	8	38	6		0	1	0	1	0	2.5	1		1	1	1	2.5	0
18	Avinash Kumar	Avinasharja2155@gmail.com	8877792725	15103111142	8	39	2		0	0	0	0	1	0.5	0.5		0	1	0.5	0.5	0
19	Alok Kumar	Alokkumar79384@gmail.com	8709069155	15103111143	8	46	6		2	0.5	0	0.5	1	0.5	1		0.5	1.5	1	0.5	2
20	Nitish Kumar	Nitish2121997@gmail.com	7549722851	15103111144	10	42	10		4.5	2	0	0	0	2.5	1		0	2	1	2.5	4.5
21	Rahul Kumar	Sahrahulgupta@gmail.com	8789392218	15103111145	8	47	5		0	1	0	1	1	1	1		1	2	1	1	0
22	Puja Kumari			15103111146	9	39	5		0	0	0	0.5	1.5	1	2		0.5	1.5	2	1	0
23	Rupesh Kumar Singh	Rupeshsingh681@gmail.com	9572799127	15103111147	8	46	10		0	1	1	1	1.5	3	2		1	2.5	2	4	0
24	Amit Kumar	Amitkumar0475@gmail.com	9576448028	15103111148	10	47	8		4	1	0	0.5	1.5	0	1		0.5	2.5	1	0	4
25	Anshu Kumari	Anshu11111996@gmail.com		15103111149	10	43	9		0	1	0	2	2	2	2		2	3	2	2	0
26	Abhimanyu Kumar Sinha	Abhimanyu12121997@gmail.com	6200395894	15103111150	10	42	10		4	1	0	0	1	2.5	1.5		0	2	1.5	2.5	4
27	Rituraj	Rituraj268raj@gmail.com	8809733684	15103111151	10	37	5		0	2	0	1.5	0	0	1.5		1.5	2	1.5	0	0
28	Priti Kumari	Pk141522@gmail.com		15103111152	8	41	7		0	1	0	1	2	1	2		1	3	2	1	0
29	Kanhaiya Kumar	Parjapatikanhaiya15@gmail.com	8409052790	15103111153	9	37	3		0	0	0	1	1	0	1		1	1	1	0	0
30	Sanjit Kumar Yadav	Krsanjit96@gmail.com	9709308932	15103111154	9	32	6		0	2.5	0	2	0	1	0.5		2	2.5	0.5	1	0
31	Sanyam Kumar	Kumar.sanyam97@gmail.com	9507281751	15103111155	9	48	11		0	2.5	1.5	2	2	1	1.5		2	4.5	1.5	2.5	0
32	Kumari Shanu Raj	Shanuraj0902@gmail.com		15103111156	10	52	17		5	0	3	2	2	3	2		2	2	2	6	5
33	Shankar Kumar	Shankar2012sagar@gmail.com	9534999111	15103111157	8	32	2		0	0.5	0	0.5	0	0	0.5		0.5	0.5	0.5	0	0
34	Vivek Kumar	Close2vivek4@gmail.com	9534542552	15103111158	9	39	1							0.5			0	0	0	0.5	0
35	Rahul Kumar	Rahul913535@gmail.com	7903622701	15103111159	10	42	17		4	3	2	2	1	3	1.5		2	4	1.5	5	4
36	Shashi Kant	Kant36152@gmail.com	7070332612	15103111160	8	39	2		0	0	0	0	0.5	0.5	0.5		0	0.5	0.5	0.5	0
37	Md. Ashraf Ansari	Asrf90066@gmail.com	82269043	15103111161	9	38	3		0	0	0	1	0.5	1	0.5		1	0.5	0.5	1	0
38	Randhir Kumar			15103111162	10	39	0										0	0	0	0	0
39	Priti Kumari	Priticute97@gmail.com	7319928091	15103111163	8	47	6		0	0	0	2	1.5	1	1		2	1.5	1	1	0
40	Bipul Chandra	bipultheboss@gmail.com	8789606446	15103111164	10	52	6		0.5	0.5	0	1	1	1	2		1	1.5	2	1	0.5
41	Rohit Kumar Mahto	Rohitsuman3890@gmail.com	8207481579	15103111165	8	46	2		0	0	0	0	0.5	0.5	0.5		0	0.5	0.5	0.5	0

42	Hemant Kumar	Hemantaryan2710@gmail.com	8405935320	15103111166	8	49	5		0	0	0	0	0	2.5	2		0	0	2	2.5	0
43	Kranti Kumari	Krantikumaridce@gmail.com	68540809961, 9060250038	15103111168	10	52	16		2	3	3	1	2	3	1.5		1	5	1.5	6	2
44	Divakar Kumar	Diwakar8235@gmail.com	8294314661	15103111170	8	44	2		0	0	0	0.5	0.5	0.5	0.5		0.5	0.5	0.5	0.5	0
45	Ranjana Bharti	Branjana.98@gmail.com	7261880293	15103111171	9	40	7		2.5	1	0	1.5	1.5	0	0		1.5	2.5	0	0	2.5
46	Rupa Kumari	Ruparaj1310@gmail.com	8292928466	15103111172	8	46	3		0	1	0	0.5	1	0	0.5		0.5	2	0.5	0	0
47	Gaurav Kharga	gauravkharga@gmail.com	7903305900	15103111173	8	37	10		0	2.5	1	2	1.5	1	1.5		2	4	1.5	2	0
48	Sunny Alok	Sunnyalok71@gmail.com	8298375975	15103111174	8	43	11		1	2	0.5	1.5	1	3	1.5		1.5	3	1.5	3.5	1
49	Tuhina Kumari	Tuhinagupta7890@gmail.com	7903373363	15103111175	10	42	11		0	2	0	2	2	3	2		2	4	2	3	0
50	Chandan Kumar Sah	Chandankumar91220@gmail.com	9122016491	15103111176	9	33	1		0	0	0	0	0	0.5	0		0	0	0	0.5	0
51	Mukesh Kumar Pandit	M4mukesh95@gmail.com	8539811832	15103111177	8	34	2		0	0.5	0	0.5	0.5	0	0.5		0.5	1	0.5	0	0
52	Rahul Kumar	Rk0908017@gmail.com	7323056159	15103111178	8	55	3		0	0.5	0	0.5	0.5	0.5	0.5		0.5	1	0.5	0.5	0
53	Ranjan Kumar	Ranjandce97@gmail.com	8539897855	15103111179	8	51	3		0	0.5	0.5	0.5	0.5	0	0.5		0.5	1	0.5	0.5	0
54	Pratima	Pratimarri1997@gmail.com	9470626699	15103111202	8	42	4		0.5	0	0	0.5	1.5	1	0.5		0.5	1.5	0.5	1	0.5
55	Pragati Niwas	Pragati0603@gmail.com	8409779165	15103111208	10	41	13		4.5	1.5	0	2	2	3	0		2	3.5	0	3	4.5
56	Pradeep Kumar Chaudhary	Pradeepkumarchaudhary848@gmail.com	9905415505	15103111209	8	44	2		0	1	0	0	0.5	0	0		0	1.5	0	0	0
57	Prabhakar Kumar	Prabhakar.k.yadav@gmail.com	9430003551	16110111901	8	45	6		0	1	0	1.5	1.5	0.5	1		1.5	2.5	1	0.5	0
58	Rupak Kumari	xyzrupak@gmail.com	9122044150, 9677060316	16110111902	8	43	3		0	0.5	0.5	0.5	0.5	0.5	0.5		0.5	1	0.5	1	0

Note: The attainment level be 50% of the full marks

	Students Scoring Greater Than 50 % of the full marks																
	Quiz/Assisngment	External Marks	Mid sem									CO1	CO2	CO3	CO4	CO5
50% of full marks	5	35	10									1	2.5	1	3	2.5
No of Students	58	46	14									31	20	32	12	12
% of students	100	79.31034483	24.1379									53.4483	34.4828	55.1724	20.68965517	20.6897
Attainment level achieved	3	3	0									3	1	3	0	0

Our attainment Criteria		
	50%	3
	40%	2
	30%	1

CO attainment												
	DA (Direct Assesment)							IDA (Indirect Assesment)		Co attainment	Target	Attainment
CO s	Internal Test(20 %)		External test (70 %)		Continous Assessment(10 %)		DA	IDA				Attained/Not Attained
	% of Students getting more than 50% of full marks	Attainment	% of Students getting more than 50% of full marks	Attainment	% of Students getting more than 50% of full marks	Attainment		Course Exit Survey	Attainment	80 % DA+ 20% IDA		
CO 1	53.45	3	79.31	3	100.00	3	3	4	3	3	2	Attained
CO 2	34.48	1	79.31	3	100.00	3	2.6	5	3	2.68	2	Attained
CO 3	55.17	3	79.31	3	100.00	3	3	3	3	3	2	Attained
CO 4	20.69	0	79.31	3	100.00	3	2.4	4	3	2.52	2	Attained
CO 5	20.69	0	79.31	3	100.00	3	2.4	4	3	2.52	2	Attained

Our attainment Criteria	50%	3
	40%	2
	30%	1

		CO-PO Matrix															Each PO DA attainment after divinding by max. attain (3) and then multipyling with respective CO attainment level												
CO	CO Attainment	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2		PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	3			1	1	1	1									3	0	0	1	1	1	1	0	0	0	0	0	0	0
CO 2	2.68	2	2	2	2	2	1										1.786666667	1.78667	1.78667	1.78667	1.78667	0.89333	0	0	0	0	0	0	0	0
CO 3	3	2	2	2	1	1				2							2	2	2	1	1	0	0	0	2	0	0	0	0	0
CO 4	2.52	3	3	3	3	2	1		2	3		2	1	2	2		2.52	2.52	2.52	2.52	1.68	0.84	0	1.68	2.52	0	1.68	0.84	1.68	1.68
CO 5	2.52	2	2	3	1	2	2	1	1	3		3	1	3	3		1.68	1.68	2.52	0.84	1.68	1.68	0.84	0.84	2.52	0	2.52	0.84	2.52	2.52

Surveys	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
Program Exit Survey	2.58	2.26	2.41	2.21	2.24	2.15	2.33	2.53	2.42	0	2.36	2.46	2.25	2.35
Alumni Feedback	2	2	-	-	2	2	3	2	3	0	2	3	-	-
Parent Feedback	2.01	-	-	-	2.25	2.15	2.15	2.13	-	1	-	2.25	-	-
Guest Lecture / Expert Lecture/ workshop Resource person Feedback	2	-	-	2	2	-	1	1	-	1	-	2	-	-
Guest Lecture / Expert Lecture/ Workshop Student Feedback	2	-	2	3	2	-	3	-	-	-	-		2	-
External Examiner Feedback	2	-	2	2	-	-	-	1	-	2	-	-	-	-
In-plant training u industry person	3	-	-	-	-	-	-	3	3	1	-	2	-	-
Industrial Visit by industry person	-	-	-	-	-	-	3	-	3	-	3	-	-	
Employer Feedback	2	2	-	-	2	-	2	3	2	3	2	2	-	-
Co-curricular activities	-	-	-	-	2	3	2	3	2	3	2	3	-	-
Extra-curricular activities	-	-	-	-	-	2.07	2.01	2.16	2.25	2.05	-	2.05	-	-
Recruiters	2	-	1	2	-	2	1	2	1	-	2	-	-	
Attainment	**2.18**	**2.09**	**1.8525**	**2.24**	**2.07**	**2.23**	**2.15**	**2.18**	**2.33**	**1.86**	**2.23**	**2.35**	**2.13**	**2.35**

Note: Program Exit Survey will be same for all the courses of a particular branch

Note: PO attainment is calculated after takin the average of the points. While dividing kindly consider only those points which will have non-zero input.

Note: The data enter against each POs is fictional just to undersatnd the actual senario but soon it will be valiated

CO	CO Attainment	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO 1	3	3.0	0.0	0.0	1.0	1.0	1.0	1.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 2	2.68	1.8	1.8	1.8	1.8	1.8	0.9	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
CO 3	3	2.0	2.0	2.0	1.0	1.0	0.0	0.0	0.0	2.0	0.0	0.0	0.0	0.0	0.0
CO 4	2.52	2.5	2.5	2.5	2.5	1.7	0.8	0.0	1.7	2.5	0.0	1.7	0.8	1.7	1.7
CO 5	2.52	1.7	1.7	2.5	0.8	1.7	1.7	0.8	0.8	2.5	0.0	2.5	0.8	2.5	2.5
PO Attainment (DA)		2.2	2.0	2.2	1.4	1.4	1.1	0.9	1.3	2.3	0.0	2.1	0.8	2.1	2.1
PO Attainment (IDA)		2.17667	2.08667	1.8525	2.242	2.07	2.22833	2.149	2.182	2.33375	1.864285714	2.226666667	2.345	2.125	2.35

Final Attainment		2.1932	2.01467	2.13583	1.59187	1.55747	1.32833	1.1658	1.4444	2.34408	0.372857143	2.125333333	1.141	2.105	2.15
PO Attainment Level		1	1	1	1	1	1	1	1	1	0	1	1	1	1
PO Attained/Not Attained		Attained	Attained	Attained	Attained	Attained	Attained	Attained	Attained	Attained	Not Attained	Attained	Attained	Attained	Attained