1 .
a. Find the maximum and minimum decimal number which can be store in 'K' bit registers in following representation.
I. Unsigned II. Signed III. 1's Complement IV 2's Complement.
b. Evaluate $(45678)_{\text{nine}}$ - $(87564)_{\text{nine}}$, using r's complement and (r-1)'s complement .
c. Explain flowchart of add and subtract operation.

2.
a. Represent -5.75_{ten} in IEEE 754 binary representation, both single and double precision.
b. Evaluate -39_{ten} X $+54_{\text{ten}}$ using Booth multiplication algorithm.

3.
a. Show the block diagram of hardware and register transfer statement of the following pseudocode.

if A[7 6] == 0 0 **then**
  $B = B + 5$
else if A[7 6] == 1 1 **then**
  $B = B - 5$
else if A[7 6] == 0 1 **then**
  $B = B - A$
else
  $B = B + A$
end if

Assume A and B are 8 bit registers, Here A [7 6] represents the 7^{th} and 6^{th} bit of register.
b. Define the following term.
I. Microoperation II. Macrooperation III. Microinstruction
IV. Microprogram.
c. Describe at least two situation where overflow occur, and how we can detect it.
4.
a. Register A holds the 10-bit binary 01 1011 0110. Determine the B operand and the logic microoperation to be performed in order to change the value in A to :
I. 10 1010 1011 II. 11 1011 1111 III. 01 0001 0100
b. Distinguish between BUN (Branch unconditional) and BSA (Branch and save return address) with the help of microoperation and one numerical example.
c. Show the flowchart of instruction and interrupt cycle.

5.
a. Show the input output configuration and with the help of figure explain how they communicate to each other.
b. Explain the types of microinstruction formate, give advantage and disadvantage of each type.
c. Explain each part of Micro-control organization.

6.
a. Distinguish between hardwired control unit and microprogrammed control unit.
b. In microprogrammed control unit how address of control memory is selected.

7. A hypothetical digital computer has a memory unit with a capacity of 8192 K words where each word is 16 bit. In ISA-32 instruction register holds 32 bit. in which one bit is used as parity bit that may be odd or even parity bit and one bit is used for addressing scheme .
a. How many bits will be available for opcode field and how many operation can be performed.
b. Draw the instruction formate and show the size of each field.
c. If **PC** holds the address of next instruction, then for what value of **PC** incremented in instruction cycle.

8. A digital computer has a common bus system for 33 registers of 64 bits each
a. If the bus is constructed with multiplexer then
I. How many selection input are there in each multiplexer ?
II. What size of multiplexers are needed ?
III. How many multiplexers are there in the bus?

b. If the bus is constructed with three-state buffer then
I. How many selection input are there in each decoder ?
II. What size of decoders are needed ?
III. How many decoders are there in the bus?
IV. How many three-state buffer are required ?

Submit on or before **Friday 26th April, 2019**

DARBHANGA COLLEGE OF ENGINEERING, DARBHANGA
Mid-Sem Examination

Computer Architecture

(EEE 6th Sem 051602)

Max Marks : 20
Max Time : 2 Hrs

Instruction:

Attempt any two question among three, all questions carry equal marks.

No any clarification related to question will be entertain, If you are considering any assumption must mention it.

1.

a. Express $-(15)_{ten}$ in One's Complement and Two's Complement representation.

b. Evaluate the range of decimal number which can store in 'K' bit register in following representation : Unsigned magnitude, Sign Magnitude, One's Complement and Two's Complement.

c. Explain the condition of overflow in addition and arithmetic left shift with example.

2+4+4 = 10

2.

a. Give the register transfer notation and hardware construction diagram of following code.

IF D[0] = 0 then
A = A + $(5)_{ten}$
ELSE
A = A – $(5)_{ten}$

where A and D are 4 bit registers.

b. Compute the content of QA register at the end of the 3rd iteration in Booth multiplication Algorithm where operands are store in A and B register and Q is initialize with zero. In A and B register stored value is binary equivalent of $-(15)_{ten}$ and $(6)_{ten}$ respectively.

5+5 = 10

3. Add the number $(0.5)_{10}$ and $-(0.4375)_{10}$ in binary using the floating point addition subtraction algorithm also gives the flowchart.

10

DARBHANGA COLLEGE OF ENGINEERING, DARBHANGA
Mid-Sem Examination

Computer Architecture

(CSE 4th Sem 051602)

Max Marks : 40
Max Time : 2 Hrs

Instruction:

Question number 1 consists of ten objective question with **negative** marking which is compulsory, in remaning question attempt any three, all questions carry equal marks.

No any clarification related to question will be entertained, If you are considering any assumption must mention it.

1. For each correct answer you will be awarded by **1** marks, each wrong answer you will be awarded by **– 0.25** and no answer you will be awarded by **0** marks. Choose the most appropriate option.

1. - 0 occurs in which representation .
   a. Sign Magnitude System. b. One's Complement representation
   c. Both a and b. d. None of these.

2. Range in decimal number of following representation is same.
   a. Unsigned magnitude representaion and Two's Complement representation.
   b. Unsigned magnitude representation and One's Complement representation.
   c. Signed magnitude representation and Two's Complement representation.
   d. Signed magnitude representation and One's Complement representation.

3. Floating point addition / subtraction is not
   a. Associative b. Commutative
   c. Both a and b d. None of these

4. During alignment of exponent in floating point left shift causes
   a. Wrong Result b. Less accuracy
   c. Both a and b d. None of these

5. Branch save return address can be implemeted using following data structure.
   a. Linked List b. Stack
   c. Queue d. All of the above

6. Which of the following micro-operation is valid.
   a. pT: AR ← $\overline{AR}$, AR ← 0 b. qT: $R_1 \leftarrow R_3$, $R_1 \leftarrow R_2$
   c. rT: PC ← AR, PC ← PC + 1 d. sT : $R_1 \leftarrow R_2$, $R_2 \leftarrow R_1$

7. Three times arithmetic shift right on binary number 10011011 will be
   a. 11110011 b. 11100110 c. 00100110 d. 00010011

8. If C_n and C_{n-1} are two contiguious carry then condition for overflow is
   a. $\overline{C_n \odot C_{n-1}} = 1$ b. $C_n \oplus C_{n-1} = 1$ c. $C_n \odot C_{n-1} = 0$ d. All of the above

9. If there are 'K' binary variables then total number of micro-operations can be
   a. 2^K b. K^2 c. 2^{2^K} d. None of these

10. Underflow exists in

a. Subtraction b. Division c. Both a and b d. None of these

2.

a. Give the register transfer notation and hardware construction for following peace of code. Assume D and A are 4 bit registers.

IF D[0] = A[3] then

$A = A + (1)_{ten}$

ELSE

$A = A - (1)_{ten}$

b. Estimate the number of muliplexer, size of multiplexer and how many selection bit in multiplexer for constructing common bus to connect 32 registers each having 64 bits.

c. Register A holds the 8 bit binary 11011001. Determine the B operand and the two logic microoperation to be perfromed in order to change the value in A to 11011111.

4+3+3 = 10

3.

a. Evaluate $-(15)_{ten}$ X $+(14)_{ten}$ using Booth multiplication algorithm.

b. In Division one of operand is in register A and other in register B, you have one more register P initialize with zero. Show that (P,A) has same bits in both restoring and nonrestornig division algorithm.

5+5 = 10

4.

a. Co-relate branch unconditional (BUN) and branch save return address (BSA) using microoperation.

b. Discuss advantage and dis-advantage of direct memory address and indirect memory address.

c. Co- relate micro-operation and macro-operation.

4+3+3=10

5.

a. Represent the number 0.5_{ten} and -0.4375_{ten} in single precision IEEE 754 representation and then evaluate 0.5_{ten} X -0.4375_{ten} using floating point multiplication.

b. A hypothetical processor having 16 MB memory, where each word in this computer is 1 byte. Assume 32 bit ISA (Instruction Set Architecture) having number of operations 16. One of operand is in mmeory and other operand is in register, there are 7 general purpose register. One bit is used as a mod bit which tells about addressing mode.

i. Draw the instruction formate and specifie each parts in number of bits.

ii. Since PC holds the address of next instruction, for addressing next instruction P C $\leftarrow$ PC + X , microinstruction must be executed. Evaluate the value of X.

5+5=10

Darbhanga College of Engineering Darbhanga

Midterm Exam, April 2019

Computer Architecture

(CSE 4th Sem 051402)

Duration: 2 Hrs **Max Marks : 20**

Regestration No:

Instruction:

1. **If any rough work found on question paper during examination, invigilator can deduct 5 marks.**
2. Attempt any four question, all questions carry equal marks.
3. No any clarification related to question will be entertained, If you are considering any assumption must mention it.

1. A digital computer has a common bus system for 33 registers of 64 bits each

a. If the bus is constructed with multiplexer then
I. How many selection input are there in each multiplexer?
II. What size of multiplexers are needed?
III. How many multiplexers are there in the bus?

b. If the bus is constructed with three-state buffer then
I. How many selection input are there in each decoder?
II. What size of decoders are needed?

$3 + 2$

2. Draw the flowchart for interrupt cycle, demonstrate it using numerical example and microoperation. Assume return address will be stored in high end[1] of memory.

5

3. A hypothetical processor having 32 MB memory. Assume 32 bit ISA[2] (Instruction Set Architecture), one bit is used as a mode bit which tells about addressing mode. One of operand is in memory and other operand is in register, there are 7 general purpose register.
a. Find the number of bits in each part of instruction register as shown in figure, how many operation can be performed?

Mode bit	Opcode	Register Select	Address Memory

b. Since PC holds the address of next instruction, for addressing next instruction PC $\leftarrow$ PC + X , instruction must be executed. Evaluate the value of X.

$3 + 2$

[1] If memory having size 1024 word, then 0^{th} word represent low end and 1023^{th} word represent high end.

[2] An instruction size is 32 bit.

4.
a. Represent the number -0.4375_{ten} in IEEE 754 representation single and double precision.
b. Give the three times arithmetic shift right on binary number 10011001.

$4 + 1$

5.
a. Draw the flowchart for add and subtract operation.
b. Compute 1234_{five} - 43210_{five} using r's complement subtraction.

$3 + 2$

6. Evaluate using Booth multiplication algorithm -31_{ten} X +17_{ten}, show each step of evaluation.

5

End