Darbhanga College of Engineering, Darbhanga

Digital Electronics

B.Tech. EEE Department

Unit 1

1. Realize F = A'B+AB' using minimum universal gates.
2. If A & B are Boolean variables and if A=1 & A+B=0, Find B?
3. Write down fan-in & fan-out of a standard TTL IC.
4. Prove that AB+A'C+BC = AB + A'C
5. Define minterm & Maxterm. Give examples.
6. What are don't care terms?
7. What are universal gates implement AND gate using any one universal gate?
8. What are the advantages of Schottky TTL family?
9. Define the term (i). Propagation delay (ii). Power dissipation
10. Draw the XOR logic using only NAND gates.
11. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.
    A. A = 1, B = 1, C = 0
    B. A = 0, B = 0, C = 0
    C. A = 1, B = 1, C = 1
    D. A = 1, B = 0, C = 1
12. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):
    A. AND
    B. NAND
    C. NOR
    D. OR
13. Determine the values of A, B, C, and D that make the sum term A'+B+C'+D equal to zero.
    A. A = 1, B = 0, C = 0, D = 0
    B. A = 1, B = 0, C = 1, D = 0
    C. A = 0, B = 1, C = 0, D = 0
    D. A = 1, B = 0, C = 1, D = 1
14. The expression for Absorption law is given by _____
    a) A + AB = A
    b) A + AB = B

c) AB + AA’ = A
d) A + B = B + A

15. According to boolean law: A + 1 = ?
a) 1
b) A
c) 0
d) A’

16. Which of the following logic families has the highest maximum clock frequency?
a) S-TTL
b) AS-TTL
c) HS-TTL
d) HCMOS

17. What causes low-power Schottky TTL to use less power than the 74XX series TTL?
a) The Schottky-clamped transistor
b) A larger value resistor
c) The Schottky-clamped MOSFET
d) A small value resistor

18. Integrated circuits are classified as _____
a) Large, Small and Medium
b) Very Large, Small and Linear
c) Linear and Digital
d) Non-Linear and Digital

19. According to the IC fabrication process logic families can be divided into two broad categories as:
a) RTL and TTL
b) HTL and MOS
c) ECL and DTL
d) Bipolar and MOS

20. CMOS refers to _____
a) Continuous Metal Oxide Semiconductor
b) Complementary Metal Oxide Semiconductor
c) Centred Metal Oxide Semiconductor
d) Concrete Metal Oxide Semiconductor

Unit 2

1. (i) Find the Minimized logic function using K-Maps and Realize using NAND and NOR gate. F (A, B, C, D) =∑ (1,3, 5,6, 7,12,14,15) .
   (ii) Show that if all the gate in a two-level OR-AND gate network are replaced by NOR gate, the output function does not change.
2. Illustrate the MSOP representation for F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26)+d(0,11,16,27) using K-map method. Draw the circuit of the minimal.
3. Write about Excess 3 and Gray Code with an example.
4. Implement F= A'B'D'+ B'C' using NAND gates.
5. What is combinational circuit? Give an example.
6. Write the procedural steps for the design of combinational circuits.
7. Define priority encoder. Give the truth table for 4 bit priority encoder.
8. Draw the Truth Table of Full Adder.
9. Draw a 1 to 2-demultiplexer circuit.
10. What is Multiplexer? Draw its block diagram and explain its working.
11. There are _____ cells in a 4-variable K-map.
    a) 12
    b) 16
    c) 18
    d) 8

12. Product-of-Sums expressions can be implemented using _____
    a) 2-level OR-AND logic circuits
    b) 2-level NOR logic circuits
    c) 2-level XOR logic circuits
    d) Both 2-level OR-AND and NOR logic circuits

13. Don't care conditions can be used for simplifying Boolean expressions in _____
    a) Registers
    b) Terms
    c) K-maps
    d) Latches

14. Half subtractor is used to perform subtraction of _____
    a) 2 bits
    b) 3 bits
    c) 4 bits
    d) 5 bits

15. Let the input of a subtractor is A and B then what the output will be if A = B?
    a) 0
    b) 1
    c) A
    d) B

16. In a combinational circuit, the output at any time depends only on the _____ at that time.
    a) Voltage
    b) Intermediate values
    c) Input values
    d) Clock pulses

17. How many outputs are present in a BCD decoder?
    a) 4
    b) 5
    c) 15
    d) 10

18. For 8-bit input encoder how many combinations are possible?
    a) 8
    b) 2^8
    c) 4
    d) 2^4

19. In 1-to-4 demultiplexer, how many select lines are required?
    a) 2
    b) 3
    c) 4
    d) 5

20. Which of the following circuit can be used as parallel to serial converter?
    a) Multiplexer
    b) Demultiplexer
    c) Decoder
    d) Digital counter

Unit 3

1. What is sequential circuit?
2. What is the difference between latch and flip flop?
3. How race around condition can be eliminated?
4. What is the application of T flip flop?
5. What is a register?
6. How many types of shift register counters are there and write their names also?
7. What is a counter?
8. What is the application of T flip flop?
9. What is the difference between asynchronous counter and synchronous counter?
10. Explain BCD counter.
11. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

12. One example of the use of an S-R flip-flop is as _____
    a) Transition pulse generator
    b) Racer
    c) Switch debouncer
    d) Astable oscillator
13. The truth table for an S-R flip-flop has how many VALID entries?
    a) 1
    b) 2
    c) 3
    d) 4
14. What is an ambiguous condition in a NAND based S'-R' latch?
    a) S'=0, R'=1
    b) S'=1, R'=0
    c) S'=1, R'=1
    d) S'=0, R'=0
15. In a NAND based S'-R' latch, if S'=1 & R'=1 then the state of the latch is _____
    a) No change
    b) Set
    c) Reset
    d) Forbidden
16. Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs?
    a) Gated JK-latch
    b) Gated SR-latch
    c) Gated T-latch
    d) Gated D-latch
17. A J-K flip-flop can be obtained from the clocked S-R flip-flop by augmenting _____
    a) Two AND gates
    b) Two NAND gates
    c) Two NOT gates
    d) Two OR gates
18. The phenomenon of interpreting unwanted signals on J and K while Cp (clock pulse) is HIGH is called _____
    a) Parity error checking
    b) Ones catching
    c) Digital discrimination
    d) Digital filtering
19. In D flip-flop, D stands for _____
    a) Distant
    b) Data

c) Desired
d) Delay

20. The D flip-flop has _____ input.
    a) 1
    b) 2
    c) 3
    d) 4

Unit-4

1. Explain the operation of basic sample and hold circuit.
2. State the advantages and applications of sample and hold circuits.
3. List the drawbacks of binary weighted resistor technique of D/A conversion.
4. Find the resolution of a 12 bit DAC converter.
5. Why does the dual slope ADC provide excellent noise rejection of AC signal whose periods are integral multiples of the integration time?
6. What are the advantages and disadvantages of R-2R ladder DAC.
7. What are the types of ADC and DAC.
8. Define start of conversion and end of conversion.
9. What is the difference between direct ADC and integrating type ADC.
10. What are the applications of 555 Timer?
11. How many control lines are present in analog to digital converter in addition to reference voltage?
    a) Three
    b) Two
    c) One
    d) None of the mentioned
12. Find out the integrating type analog to digital converter?
    a) Flash type converter
    b) Tracking converter
    c) Counter type converter
    d) Dual slope ADC
13. Which type of ADC follow the conversion technique of changing the analog input signal to a linear function of frequency?
    a) Direct type ADC
    b) Integrating type ADC
    c) Both integrating and direct type ADC
    d) None of the mentioned
14. Which A/D converter is considered to be simplest, fastest and most expensive?
    a) Servo converter
    b) Counter type ADC
    c) Flash type ADC
    d) All of the mentioned

15. The flash type A/D converters are called as
    a) Parallel non-inverting A/D converter
    b) Parallel counter A/D converter
    c) Parallel inverting A/D converter
    d) Parallel comparator A/D converter
16. What is the advantage of using flash type A/D converter?
    a) High speed conversion
    b) Low speed conversion
    c) Nominal speed conversion
    d) None of the mentioned
17. The number of comparator required for flash type A/D converter
    a) Triples for each added bit
    b) Reduce by half for each added bit
    c) Double for each added bit
    d) Doubles exponentially for each added bit
18. Drawback of counter type A/D converter
    a) Counter clears automatically
    b) More complex
    c) High conversion time
    d) Low speed
19. Calculate the conversion time of a 12-bit counter type ADC with 1MHz clock frequent to convert a full scale input?
    a) 4.095 μs
    b) 4.095ms
    c) 4.095s
    d) None of the mentioned
20. In a servo tracking A/D converter, the input voltage is greater than the DAC output signal at this condition
    a) The counter count up
    b) The counter countdown
    c) The counter back and forth
    d) None of the mentioned

Unit-5

1. Give the classification of semiconductor memories.
2. Implement the following function using PLA F1=$\sum$ (2, 4, 5, 10, 12, 13, 14) and F2 = $\sum$ (2, 9, 10, 11, 13, 14, 15).
3. Realized BCD to Excess-3 code using ROM array.
4. Realize the following function using PLA F (w, x, y, z) = Π (0, 3, 5, 7, 12, 15) + d (2, 9). Write short note on RAM, types of ROMs.
5. Implement the following function using PLA F1=$\sum$ (0, 1, 2, 4) and F2 = $\sum$ (0, 5, 6, 7).

6. Realize the following function using PAL F1(x, y, z) = ∑ (1, 2, 4, 5, 7). And F2(x, y, z) = ∑ (0, 1, 3, 5, 7).
7. Write a note on FPGA with neat diagram.
8. Explain read cycle and write cycle timing parameter with the help of timing diagram.
9. Design a combinational circuit using ROM. The circuit accepts a three bit number and outputs a binary number equal to the square of the input number.
10. How can one make 64X8 ROM using 32X4 ROMs? Draw such a circuit & explain.
11. Which of the following has the capability to store the information permanently?
    a) RAM
    b) ROM
    c) Storage cells
    d) Both RAM and ROM
12. ROM has the capability to perform _____
    a) Write operation only
    b) Read operation only
    c) Both write and read operation
    d) Erase operation
13. The MOS technology based semiconductor ROMs are classified into _____ categories.
    a) 2
    b) 3
    c) 4
    d) 5
14. MOS ROM is constructed using _____
    a) FETs
    b) Transistors
    c) MOSFETs
    d) BJTs
15. The full form of EEPROM is _____
    a) Erasable Electrically Programmable ROMs
    b) Electrically Erasable Programmable ROMs
    c) Electrically Erasable Programming ROMs
    d) Electrically Erasable Programmed ROMs
16. Which programming is done during manufacturing process?
    a) Mask Programming
    b) PROM
    c) Both PROM and mask programming
    d) EPROM
17. ROM may be programmed in _____ ways.
    a) 2
    b) 3

c) 4
d) 5

18. A photographic negative is called a _____
    a) Photo
    b) Negative
    c) Mask
    d) Virtual image
19. The memory capacity of a static RAM varies from _____
    a) 32 bit to 64 bit
    b) 64 bit to 1024 bit
    c) 64 bit to 1 Mega bit
    d) 512 bit to 1 Mega bit
20. The input data bit is written into the cell by setting _____
    a) The flip-flop for 1
    b) Resetting the flip-flop
    c) The flip-flop for HIGH
    d) Both the flip-flop for 1 and resetting the flip-flop